In the Claims:

1   **Please amend Claim 1 as follows.**

2

3   1.   (Three Times Amended) A data processing system

4   comprising:

5   a communication bus;

6   a ~~master-state~~ plurality of data processing ~~unit~~

7   units, the data processing units including:

8   ~~a communication bus, the master-state data processing~~

9   ~~unit exchanging asynchronous transfer mode protocol signals~~

10   ~~with the bus; and~~

11   ~~at least one slave-state data processing unit, the~~

12   ~~slave-state data processing unit including:~~

13   a central processing unit;

14   a direct memory access unit coupled to the

15   central processing unit, and

16   a Utopia mode interface unit coupled to the

17   direct memory access unit, the Utopia interface unit acting

18   in a receive mode and in a transmit mode; the Utopia

19   transfer mode interface unit having:

20   a processor coupled to the communication bus

21   and exchanging asynchronous transfer mode protocol signals

22   therewith; and

1   a buffer memory unit, the buffer memory unit

2   buffering data signals between the direct memory access

3   unit and the processor, ~~wherein the transfer of data cells~~

4   ~~between the buffer memory unit and the direct memory~~

5   ~~interface unit is determined by an event signal, the event~~

6   ~~signal indicating to the direct memory access unit that a~~

7   ~~data cell is stored in the buffer memory unit in the~~

8   ~~receive mode, the event signal indicating to the direct~~

9   ~~memory access unit that space for a data cell is available~~

10   ~~in buffer memory unit in the transmit mode~~;

11   <u>wherein one of the data processing units operates in a</u>

12   <u>master mode and the remainder of the data processing units</u>

13   <u>operate in a slave mode.</u>

14

15   2.   (Previously Cancelled)   ~~The data processing~~

16   ~~system as recited in claim 1 wherein the Utopia interface~~

17   ~~unit can act in a receive mode and in a transmit mode.~~

18

19   3.   (Original)   The data processing system as

20   recited in claim 1 wherein the buffer memory unit is a

21   first-in/first-out memory unit.

22

23   4.   (Original)   The data processing system as

24   recited in claim 1 wherein the processor includes:

25   an input interface unit; and

26   an output interface unit; and wherein the buffer

27   memory unit includes:

1   an input buffer memory unit, wherein the transfer

2   between the input buffer memory unit and the direct memory

3   access unit is determined by a receive event signal; and

4   an output buffer memory unit, wherein the transfer

5   between the direct memory access unit and the output buffer

6   memory unit is determined by a transmit event signal.

7

8   5.   (Original)   The data processing system as

9   recited in claim 4 wherein data is transferred from the

10   communication bus to the input buffer memory unit, and

11   wherein data is transferred from the output buffer memory

12   unit to the communication unit through the output interface

13   unit.

14

15   6.   (Original)   The data processing system as

16   recited in claim 5 wherein in the input buffer memory unit

17   and the output buffer memory units are first-in/first-out

18   memory units.

19

20   7.   (Original)   The data processing system as

21   recited in claim 4 wherein the receive event signal is

22   generated when the buffer memory unit has a complete data

23   cell stored therein, the receive event signal being cleared

24   when transfer between the buffer memory unit and the direct

25   memory access unit is begun, and wherein the transmit event

26   signal is generated when the buffer memory unit has space

1   for a complete data cell, the transmit event signal being

2   cleared when the transfer of the data cell to the buffer

3   memory unit from the direct memory access unit is begun.

4

5   **Please amend Claim 8 as follows.**

6

7   8.   (Three Times Amended)   A data processing system

8   ~~comprising:~~ including ~~at least one slave-state data~~

9   ~~processing unit;~~ a communication bus ~~the master-state data~~

10   ~~processing unit~~ for exchanging asynchronous transfer mode

11   protocol signals, ~~with the bus;~~ and a ~~master-state~~

12   plurality of data processing ~~unit~~ units, the ~~master-state~~

13   data processing ~~unit including~~ units having:

14   a central processing unit;

15   a direct memory access unit coupled to the central

16   processing unit, and

17   a Utopia interface unit coupled ~~to~~ between the direct

18   memory access unit; the Utopia interface unit ~~having~~

19   comprising:

20   a processor coupled to the communication bus

21   and exchanging asynchronous transfer mode protocol signals

22   therewith; and

23   a buffer memory unit, the buffer memory unit

24   buffering data signals between the direct memory access

25   unit and the processor, an event signal indicating to the

26   direct memory access unit when a data cell has been

1 received by the buffer memory unit in a receive mode, an

2 event signal indicating to the direct memory access unit

3 that space for a data cell is available in the receive

4 mode;

5   wherein the UTOPIA interface unit can send and receive

6 signals in either the master-mode or the slave-mode.

7

8   9.   (Original)   The data processing system as

9 recited in claim 8 wherein the processor includes:

10   an input interface unit; and

11   an output interface unit: and wherein the buffer

12 memory unit includes;

13   an input buffer memory unit; and

14   an output buffer memory unit.

15

16   10. (Original)   The data processing system as

17 recited in claim 9 wherein the data is transferred from the

18 communication bus through the input interface unit to the

19 input buffer memory unit, and wherein data is transferred

20 from the output buffer memory unit through the output

21 interface unit to the communication bus.

22

23   11. (Original)   The data processing system as

24 recited in claim 10 wherein the input buffer memory unit

1   and the output buffer memory unit are first-in/first-out

2   memory units.

3

4   **Please amend Claim 12 as follows:**

5

6   12.   (Twice Amended)   An Utopia interface unit for

7   providing an interface between an external data processing

8   unit and a direct memory access unit, the interface unit

9   comprising:

10   an input buffer memory unit, the input buffer memory

11   unit providing data cells to the direct memory interface

12   unit, the input buffer unit applying an event signal to

13   direct memory access unit indicating that space is

14   available for a data cell in a transmit mode, the ~~inp9ut~~

15   input buffer applying an event signal to the direct memory

16   access unit indicating that data cell is stored therein in

17   a receive mode;

18   an interface input unit, the interface input unit

19   controlling the transmission of data cells from the

20   external processing system to the input buffer memory unit;

21   an output buffer memory unit, the output buffer memory

22   unit receiving data cells from the direct memory access

23   unit; and

24   an interface output unit, the interface output unit

25   controlling transmission of data cells from the output

26   buffer memory unit to the external processing system<u>;</u>

1   wherein the interface unit can operate in either a

2 master-mode or a slave mode with respect to the external

3 data processing unit.

4

5   13. (Original) The interface unit as recited in

6 claim 12 wherein the input buffer memory unit and the

7 output buffer memory unit are first-in/first-out memory

8 units.

9

10   14. (Original) The interface unit as recited in

11 claim 12 wherein the first-in/first-out memory units can

12 store at least two data cells.

13

14   15. (Original) The interface unit as recited in

15 claim 12 wherein data from the input buffer memory unit is

16 transferred to the direct memory access unit in response to

17 word-read signal from the buffer memory unit.

18

19   16. (Original) The interface unit as recited in

20 claim 12 wherein data from the direct memory unit is stored

21 in the output buffer memory unit in response to a word-

22 write signal from the output buffer memory unit.

23

24   17. (Original) The interface unit as recited in

25 claim 12 wherein data is transferred from the external

1 processing unit to the input buffer unit in response to the
2 cell-available signal from the input buffer unit.

3

4   18. (Original)   The interface unit as recited in
5 claim 12 wherein data is transferred from the output buffer
6 memory unit to the external processing unit in response to
7 the cell-available signal from the output buffer memory
8 unit.
9

10   19. (Original)   The interface unit as recited in
11 claim 12 wherein the interface unit is operating in a slave
12 mode, the transfer of data cells from the input buffer
13 memory unit and the direct memory access unit being
14 determined by a receive event signal, the transfer of data
15 cells from the direct memory access unit to the output
16 buffer memory unit being determined by a transmit event
17 signal.

18

19   20. (Original)   The data processing system as
20 recited in claim 19 wherein the receive event signal is
21 generated when the input buffer memory unit has a complete
22 data cell stored therein, the receive event signal being
23 cleared when transfer between the input buffer memory unit
24 and the direct memory access unit is begun, and wherein the
25 transmit event signal is generated when the output buffer
26 memory unit has space for a complete data cell, the
27 transmit event signal being cleared when the transfer of

1   the data cell to the output buffer memory unit from the

2   direct memory access unit is begun.

3

4   **Please cancel Claim 21.**

5

6   21. (Currently Cancelled) ~~The data processing~~

7   ~~system as recited in claim 12 wherein the receive event~~

8   ~~signal is generated when the buffer memory unit has a~~

9   ~~complete data cell stored therein, the receive event signal~~

10   ~~being cleared when transfer between the buffer memory unit~~

11   ~~and the direct memory access unit is begun, and wherein the~~

12   ~~transmit event signal is generated when the buffer memory~~

13   ~~unit has space for a complete data cell, the transmit event~~

14   ~~signal being cleared when the transfer of the data cell to~~

15   ~~the buffer memory unit from the direct memory access unit~~

16   ~~is begun.~~

17

18   **Please add Claim 22.**

19   22. (Newly Added) <u>The data processing system of claim</u>

20   <u>1 wherein the transfer of data cells between the buffer</u>

21   <u>memory unit and the direct memory interface unit is</u>

22   <u>determined by an event signal, the event signal indicating</u>

23   <u>to the direct memory access unit that a data cell is stored</u>

24   <u>in the buffer memory unit in the receive mode, the event</u>

25   <u>signal indicating to the direct memory access unit that</u>

26   <u>space for a data cell is available in buffer memory unit in</u>

27   <u>the transmit mode.</u>